Vivado Simulator 2017.3

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Running: C:/Xilinx/Vivado/2017.3/bin/unwrapped/win64.o/xelab.exe -wto 84a0f0b44b4c401cbb80523fe79ddc16 --incr --debug typical --relax --mt 2 --maxdelay -L xil\_defaultlib -L simprims\_ver -L secureip --snapshot Testbench\_full\_adder\_time\_impl -transport\_int\_delays -pulse\_r 0 -pulse\_int\_r 0 -pulse\_e 0 -pulse\_int\_e 0 xil\_defaultlib.Testbench\_full\_adder xil\_defaultlib.glbl -log elaborate.log

Using 2 slave threads.

Starting static elaboration

Completed static elaboration

Starting simulation data flow analysis

Completed simulation data flow analysis

INFO: [XSIM 43-3451] SDF backannotation process started with SDF file "Testbench\_full\_adder\_time\_impl.sdf", for root module "Testbench\_full\_adder/uut".

INFO: [XSIM 43-3452] SDF backannotation was successful for SDF file "Testbench\_full\_adder\_time\_impl.sdf", for root module "Testbench\_full\_adder/uut".

Time Resolution for simulation is 1ps

Compiling package std.standard

Compiling package std.textio

Compiling package ieee.std\_logic\_1164

Compiling package ieee.std\_logic\_arith

Compiling package ieee.std\_logic\_unsigned

Compiling package vl.vl\_types

Compiling module xil\_defaultlib.glbl

Compiling module simprims\_ver.IBUF

Compiling module simprims\_ver.OBUF

Compiling module simprims\_ver.x\_lut3\_mux8

Compiling module simprims\_ver.LUT3

Compiling module xil\_defaultlib.full\_adder

Compiling architecture behavior of entity xil\_defaultlib.testbench\_full\_adder

Built simulation snapshot Testbench\_full\_adder\_time\_impl